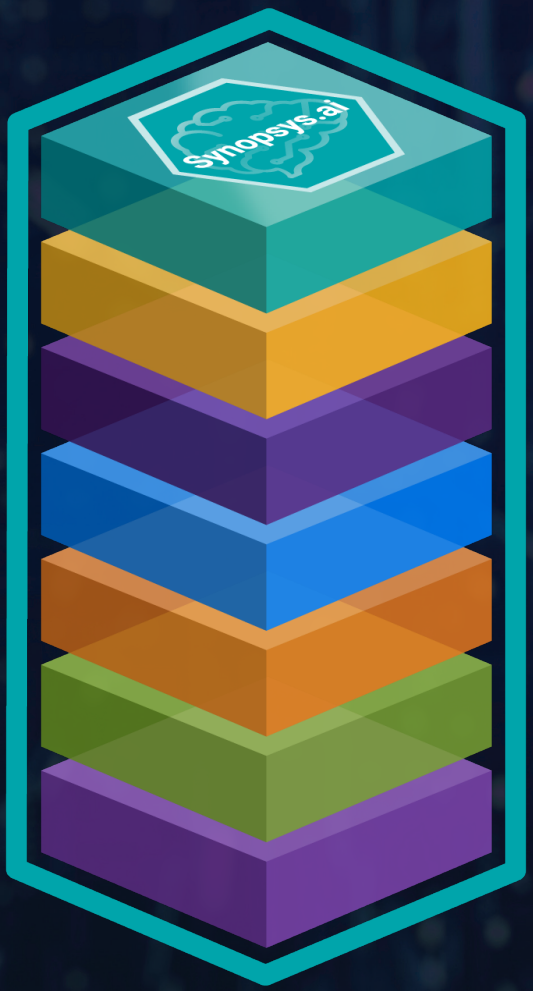
SYNOPSYS®

# Synopsys.ai – Full Stack, AI-Driven EDA Suite

## From System Architecture to Design and Manufacturing



# Overview

The rapid and exponential increase in chip design complexity is creating significant hurdles for the semiconductor industry. Companies must contend with not only challenges posed by the march to angstroms, multi-die integration, and rapid node migration, but also aggressive time-to-market targets, increasing manufacturing test costs, and the global engineering resource crunch. Advancements in artificial intelligence (AI) for electronic design automation (EDA) can address these challenges head on.

Synopsys.ai™, the industry's first full stack, AI-driven electronic design automation (EDA) suite, is delivering significant quality of results (QOR) and productivity improvement across implementation, verification, and test. Synopsys.ai frees up engineers to focus on chip quality and differentiation and empowers engineers to get the right chip with the right specs to market faster.

Design engineers looking to reach the best power, performance, and area (PPA) targets can utilize the Synopsys Design Space Optimization (DSO.ai) solution. Verification engineers can achieve higher quality verification coverage faster with the Synopsys Verification Space Optimization (VSO.ai) solution. Test engineers faced with the challenge of reducing the number of test patterns while optimizing defect coverage can employ the Synopsys Test Space Optimization (TSO.ai) solution.

## Design Space Optimization—DSO.ai

Complexity brought on by advanced process nodes have opened the door to challenges in achieving optimal power, performance, and area. Manual methods are no longer viable given shrinking market windows. The need to drive for better results faster is increasing and traditional methods cannot keep pace often resulting in months of tuning using 100s of trials. Even then, results are not optimal. Synopsys DSO.ai can help.

Synopsys DSO.ai, the industry's first autonomous artificial intelligence application for chip design, searches for optimization targets in very large solution spaces of chip design, utilizing reinforcement learning to enhance power, performance, and area. RTL-to-GDSII full flow optimization unlocks PPA potential across both logical and physical domains. Breakthrough reinforcement learning engines can explore trillions of design recipes. These models continue to train and accelerate convergence throughout the design cycle and bleed over to impact efficiency and productivity on iterative designs.


Figure 1: DSO.ai provides unbeatable PPA results and the fastest time to design

Synopsys DSO.ai is an industry award-winning solution deployed by 9 out of 10 semiconductor companies. Users have reported productivity enhancements of more than 3x, power reductions of up to 15%, and substantial die size reductions. DSO.ai helps companies surpass the most challenging goals in chip design and reach new levels of productivity.

## Verification Space Optimization—VSO.ai

Logic and functional issues that undermine the readiness of SoCs require extensive verification that can quickly evolve into an endless verification and debug loop. Chip verification engineers need to check each of the design state spaces to ensure that the final SoC design will work. The number of design state spaces in which a digital design can operate is nearly infinite, making it virtually impossible for humans to check each of these spaces to validate that the design will function as intended. Achieving full verification coverage is a daunting if not impossible task using traditional methods.

The traditional coverage closure flow requires verification engineers to manually define coverage and stimulus, often running 1000's of regressions with unknown ROI. After collecting the coverage data, manual analysis of the enormous data set only leads to minimal insights. To close coverage, tests must be manually biased or directed tests must be written which is labor intensive and slow and can still lead to bug escapes.

Synopsys VSO.ai revitalizes the coverage process by using AI to examine the RTL and infer coverage while also highlighting areas where coverage is needed, ultimately helping verification engineers reach coverage targets faster and find more bugs. Regressions are optimized so high ROI tests are run first and analysis is automated to define prescribed insights. Customers report achieving up to 10x improvement in reducing functional coverage holes and up to 30% increase in IP verification productivity using AI-driven verification with Synopsys VCS® functional verification solution.

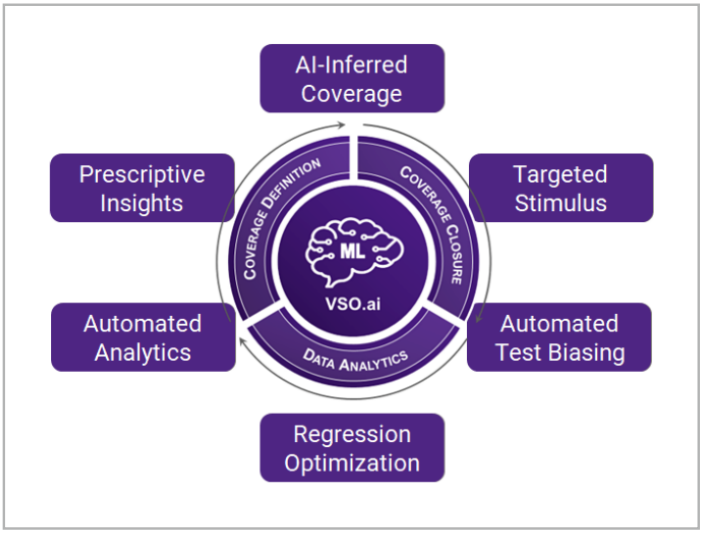



Figure 2: VSO.ai delivers faster, higher coverage closure and analytics

## Test Space Optimization—TSO.ai

Growing design complexity and size also weigh down the silicon test process. Defect coverage, pattern count (which correlates directly to testing cost), and runtime are three key metrics to consider when evaluating the results from an automatic test pattern generation (ATPG) tool.

Traditionally, optimizing for one of these metrics (typically by hand) negatively impacts the others. Someone who is new to ATPG may not have a strong sense of how to tweak the tool to generate the desired program results. Conversely, someone with a lot of experience may have biases that cause tool set up to achieve a certain result, which may not prove optimal for a new design.

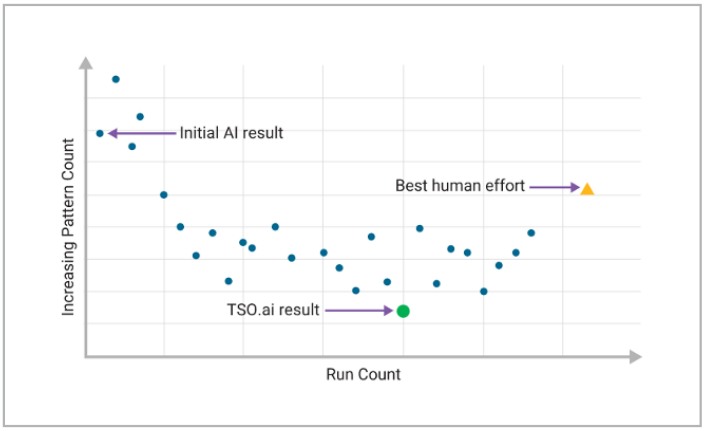



Figure 3: Optimal pattern count achieved using TSO.ai

Synopsys TSO.ai is the industry's first autonomous AI application for semiconductor test to minimize test costs and time-to-market for today's complex designs. TSO.ai automatically searches for an optimal solution in a large test search space to minimize pattern count and ATPG turn-around time reducing test costs dramatically and accelerating time to results.

Synopsys.ai EDA suite uses the power of AI to optimize silicon performance, accelerate chip design, and improve efficiency throughout the entire EDA flow. Synopsys.ai suite quickly handles design complexity and takes over repetitive tasks such as design space exploration, verification coverage and regression analytics, and test program generation, while helping to optimize power, performance, and area. This frees up engineers to focus on chip quality and differentiation. AI capabilities can help teams quickly migrate their chip designs from foundry to foundry or from process node to process node. Spend more time innovating and less time getting to market.